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10/523,257	01/27/2005	Elstan Anthony Fernandez	INF 2002 P 05725 US	8306

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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,257	FERNANDEZ, ELSTAN ANTHONY	
	Examiner	Art Unit	
	THANH Y. TRAN	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,9,15-17,19-23,25 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-6, 9, 15-17, 19-23, 25-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The indicated allowability of claims 21-22 is withdrawn in view of the newly discovered reference(s) to Chen et al (U.S. 6,472,741). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4-5, 9, 19-22, 23, 25-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen et al (U.S. 6,472,741).

As to claim 1, Chen et al discloses in figures 3C-7a semiconductor package including a substrate, an integrated circuit (320) mounted on the substrate (300), the integrated circuit (320) inherently including a plurality of IO pads on the top surface of 320 corresponding to wiring 340; a heat conductive plate ("heat spreader" 330) having a first portion including a central region interposed between the integrated circuit (320) and the substrate (300), the central region heat-conductively connected to the integrated circuit (320) and the heat conducting plate (330) having at least one second portion (as indicated at 331) extending laterally out from the central region between the integrated circuit (320) and the substrate (300), the second portion (as indicated at 331) including arms extending laterally from the central region with openings (333) between them, the integrated circuit (320) being connected to the substrate (300) by wire bonding (340) in

the openings (333), the heat conductive plate (330) being electrically isolated from the IO pads (inherently on top surface of 320 corresponding to wiring 340) of the integrated circuit (320); and a second integrated circuit (310) disposed between the plate (330) and the substrate (300), the second integrated circuit (310) including a plurality of IO pads (inherently on the bottom surface of 310 corresponding to bumps 311), the plate (330) being in heat-conductive contact with the second integrated circuit (310) but being electrically isolated from the IO pads of the second integrated circuit (310), whereby heat generated by the second integrated circuit (310) is conducted away from the second integrated circuit (310) by the plate (330).

As to claims 4 and 22, Chen et al discloses in figures 3C-7 a semiconductor package including a substrate, wherein the integrated circuit (320) has a substantially rectangular profile and wherein at least one of the arms (as indicated at 331) extends in a direction which is diagonal relative to the rectangular profile of the integrated circuit (320).

As to claims 5 and 26, Chen et al discloses in figures 3C-7 a semiconductor package including a substrate, wherein the plate (330, figure 6) is electrical grounded and electrically connected to at least one ground input (345) of the integrated circuit (320) (see col. 5, lines 1-10).

As to claim 9, Chen et al discloses in figures 3C-7 a semiconductor package in which the second integrated circuit (310) is a flipchip.

As to claim 19, Chen et al discloses in figures 3C-7 a packaged semiconductor device, further comprising a plurality of balls (360) disposed on a lower surface of the substrate (300), each of the balls (360) electrically coupled to a respective one of the contact regions (the contact regions inherently on the lower surface of substrate 300 corresponding to balls 360).

As to claim 20, Chen et al discloses in figures 3C-7 a packaged semiconductor device, wherein the central portion of the heat conductive plate (330) is affixed to the integrated circuit (320) by heat-conductive glue (321) (see col. 4, lines 38-50) and wherein the central portion of the heat conductive plate (330) is affixed to the substrate (300) by heat-conductive glue (see element 335, figure 5).

As to claim 21, Chen et al discloses in figures 3C-7 a semiconductor package including: a substrate (300); an integrated circuit (320) mounted on the substrate (300); a heat conductive plate (330) having a first portion (central portion of 330) interposed between the integrated circuit (320) and the substrate (300), the heat conductive plate (330) being heat-conductively connected to, and electrically isolated from, the integrated circuit (320) and having at least one second portion (as indicated at 331) extending laterally out from between the integrated circuit (320) and the substrate (300); and a second integrated circuit (310) disposed between the plate (330) and the substrate (300), the plate (330) being in heat-conductive contact with the second integrated circuit (310), whereby heat generated by the second integrated circuit (310) is conducted away from the second integrated circuit (310) by the plate (330); wherein the plate (330) includes a central region disposed between the substrate (300) and the integrated circuit (320) and arms extending laterally from the central region with openings (333) between them, the integrated circuit (320) being connected to the substrate (300) by wire bonding (340) in the openings (333).

As to claims 23 and 25, Chen et al discloses in figures 3C-7a semiconductor package, wherein the plate (330) further comprises an attachment to attach to a heat dissipation device (370, figure 7).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al Chen et al (U.S. 6,472,741) in view of Ahn et al (U.S. 2002/0121680).

As to claim 2, Chen et al discloses in figures 3C-7a semiconductor package in which the integrated circuit (320) is encased in resin (350, figure 3D), whereby heat generated in the integrated circuit (320) is conducted out of the resin (350).

Chen et al does not disclose the plate extending out of the resin.

Ahn et al discloses in figure 3b a semiconductor package comprising a plate (112, 110, 116a, 116b) extending out of the resin ("epoxy molding compound" 126). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the package of Chen et al by having a plate that extends out of the resin as taught by Ahn et al for strongly providing heat dissipation from the integrated circuits and/or providing an electrical connection to the substrate.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (U.S. 6,472,741) in view of Ohsawa et al (U.S. 2002/0031862).

As to claim 6, Chen et al does not disclose the plate includes at least one portion of increased thickness laterally outward from the integrated circuit.

Ohsawa et al discloses in figures 2A-2D a semiconductor package comprising a plate (comprising elements 2 and 3) includes at least one portion (3) of increased thickness laterally outward from the integrated circuit ("LSI chip" 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor package of Chen et al by having a plate that includes at least one portion of increased thickness laterally outward from the integrated circuit as taught by Ohsawa et al for supporting the semiconductor package when the semiconductor package is mounted a motherboard.

7. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (U.S. 6,472,741) in view of Araki et al (U.S. 6,828,661).

A to claims 15-17, Chen et al does not disclose the packaged semiconductor device, wherein the heat conductive plate further comprises a rim portion that surrounds the central portion and is thermally connected to the central portion by the plurality of arms, the heat conductive plate includes four diagonal arms, each diagonal arm extending outwardly from a corner of the central portion to the rim portion; and the heat conductive plate further includes four lateral arms, each lateral arm extending outwardly from a side surface of the central portion of the plate to the rim portion.

Araki et al discloses in figure 2a a packaged semiconductor device, wherein the heat conductive plate (13) comprises a rim portion (13a) that surrounds the central portion (23b) and is thermally connected to the central portion (23b) by the plurality of arms (23c), the heat conductive plate (13) includes four diagonal arms (23c), each diagonal arm (23c) extending

outwardly from a corner of the central portion (23b) to the rim portion (13a); and the heat conductive plate (13) further includes four lateral arms (23c), each lateral arm (23c) extending outwardly from a side surface of the central portion (23b) of the plate to the rim portion (13a). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Chen et al by including a rim portion that surrounds the central portion as taught by Araki et al for providing a sufficient mechanical strength or reliability of the resin-sealed semiconductor device (see col. 7, lines 32-59 in Araki et al).

Response to Arguments

8. Applicant's arguments with respect to claims 1-2, 4-6, 9, 15-17, and 19-23, and 25-26 have been considered but are moot in view of the new ground(s) of rejection.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao Le, can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/T. Y. T./
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892